HANYANG UNIVERSITY

HY-SDR RESEARCH CENTER
Hangyang Software Defined Radio Research Center

IMPLEMENTATION OF SDR-BASED WCDMA AIR PROTOCOL ANALYZER WITH AN EQUALIZER FOR SOFTWARE MODEM

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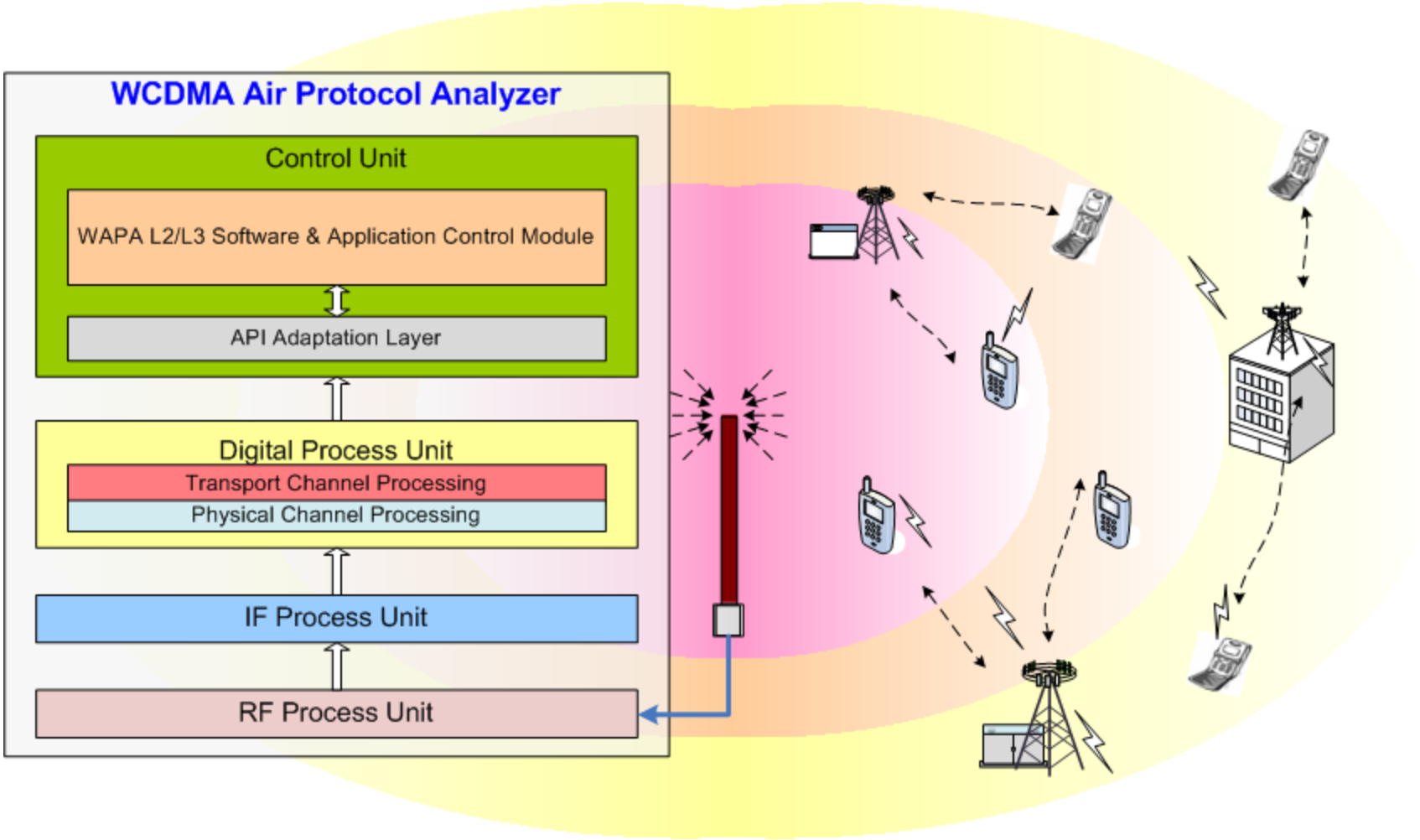
- Conclusion

- Introduction

- WCDMA Air Protocol Analyzer

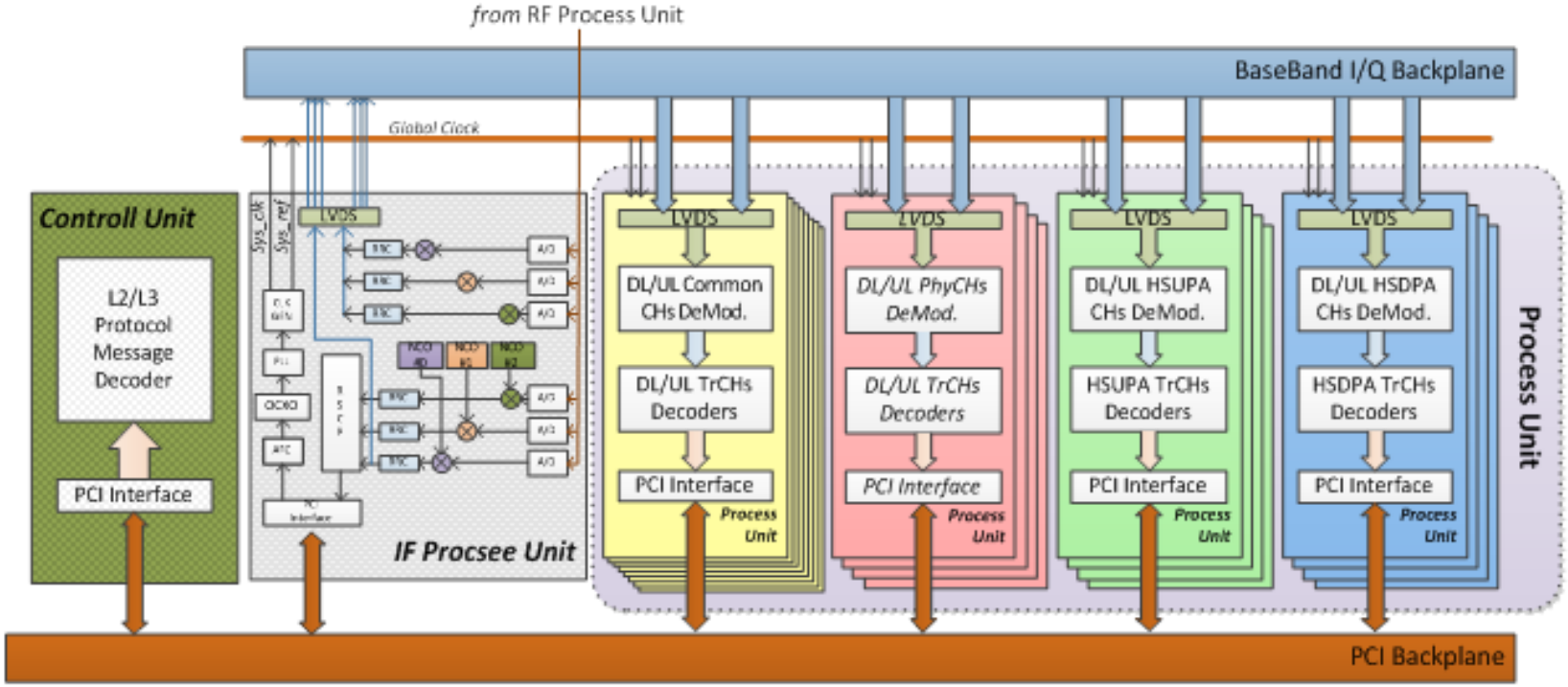


- Introduction

- For SDR architecture, The proposed system adopts standard DSPs and FPGAs
  - cPCI Processor Blade: 6U CompactPCI® Dual Quad-Core Intel® Xeon™ Processor Blade
    - ➔ L2/L3 Software & Application control module
  - Control FPGA for interface signaling of backplane bus: EP3C120F780C8
  - cPCI DSP: TMS320C6416-1GHz
  - FPGA for decoding physical channels: ALTERA EP4SE530H35C4
  - DSP for decoding transport channels: TMS320C6455

- Structure of Implemented System

- The Hardware platform consist of Radio frequency Process Unit(RPU), Intermediate frequency Process Unit(IPU), Digital Process Unit(DPU), Control Unit(CU)



- Structure of Implemented System

- Radio frequency Process Unit(RPU)
  - Support 3FAs for UL/DL respectively.
  - Down converts RF signal into IF signal and the analog IF signal is transferred to WIPU.

- Intermediate frequency Process Unit(IPU)
  - Converts the received UL/DL IF signal from RPU into baseband signals
  - Transfers the baseband signal to each processing unit
  - Cell Searching : Primary/Secondary Synchronization, acquisition of Scramble Code Number
  - Automatic Frequency Control, Automatic Gain control and
  - RSCP measurement
  - Transfers the baseband signal to the external storage through gigabit Ethernet

- Structure of Implemented System

- Digital Process Unit(DPU)
  - Consists of 3 FPGAs and 3 DSPs.

  - Control FPGA

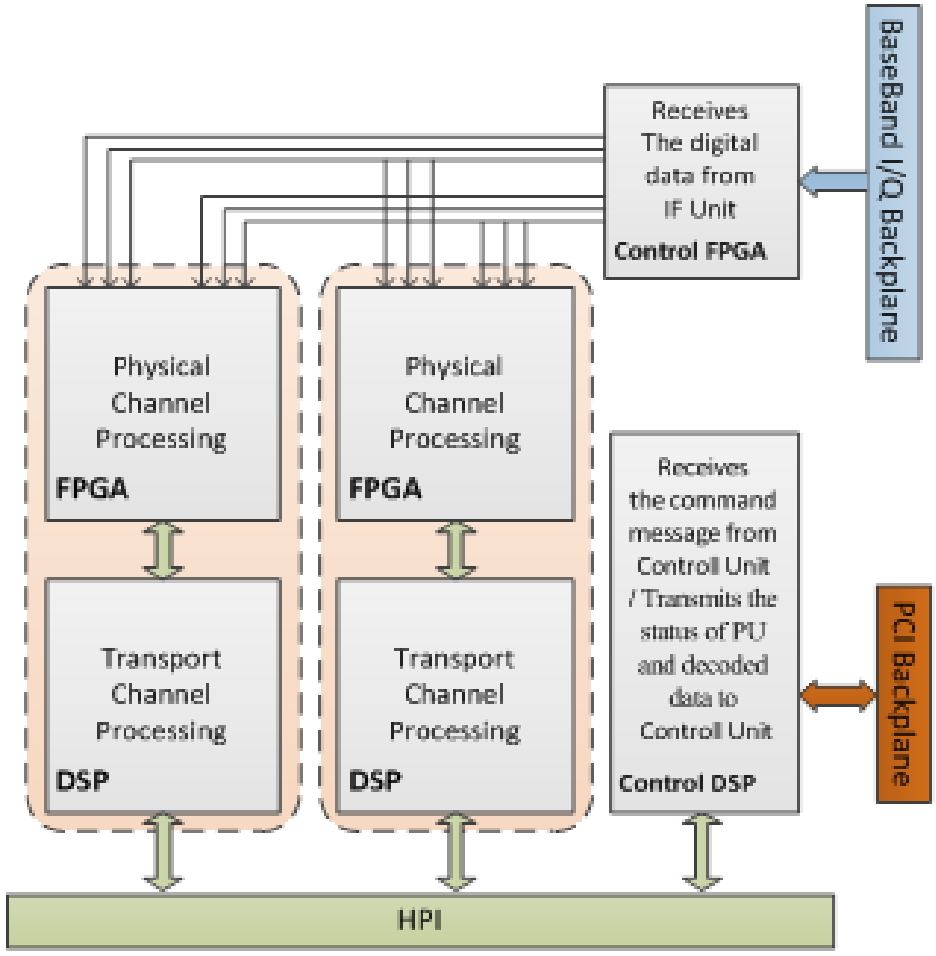
  - receives the digital data from IPU

  - Control DSP

  - receives the command message from CU
  - transmits the status of DPU and decoded data to CU through cPCI

  - 2 Pairs of FPGA and DSP

  - A FPGA demodulates a physical channel
  - A DSP decodes a transport channel



- Structure of Implemented System

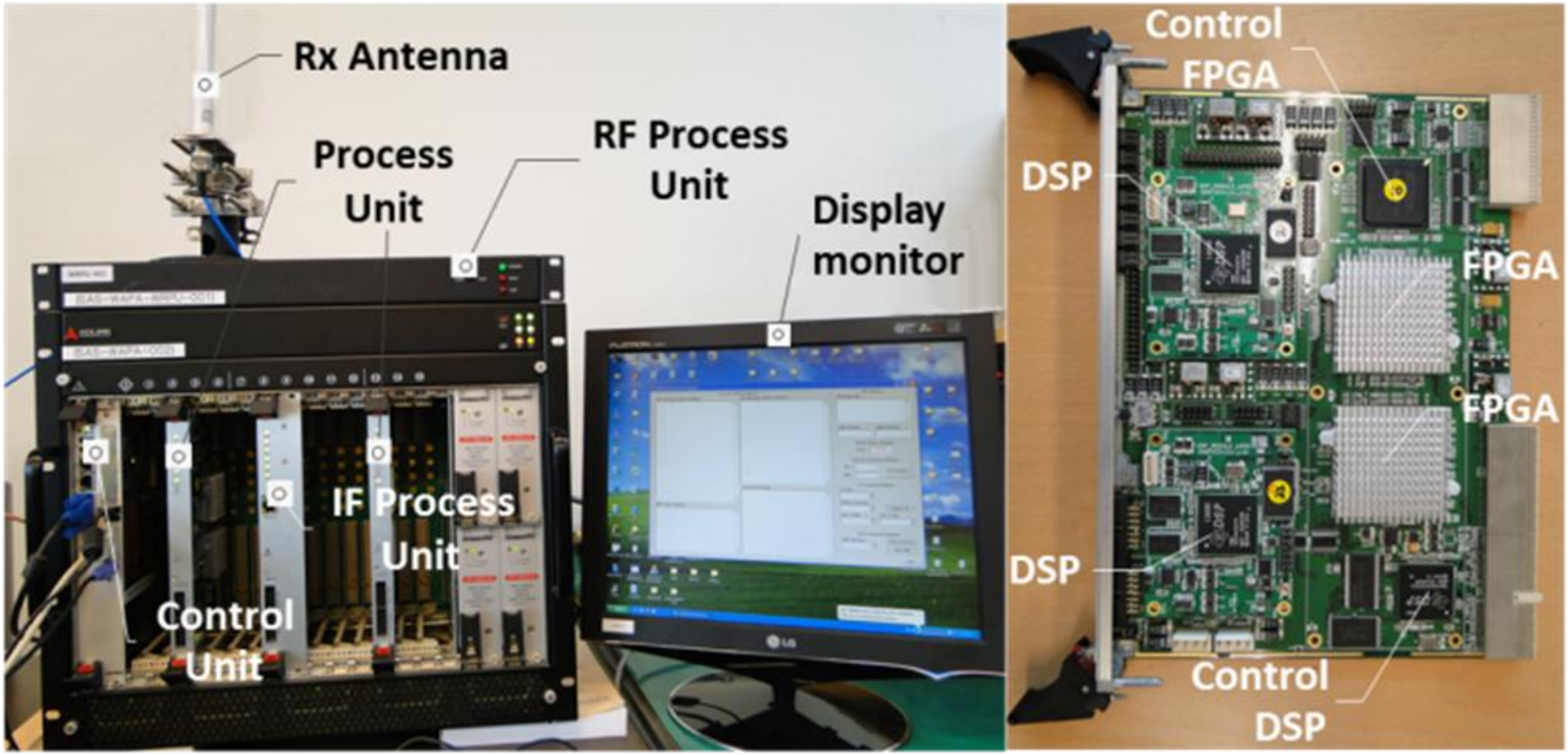
- Control Unit(CU)
  - Support data and control exchange between the PHY layer and WAPA L2/L3 software & application control module. Through API adaptation layer.
  - Using PC board : cPCI-6920D(6U CompactPCI Dual-Core Intel Xeon Processor Blade) of ADLINK Technology Inc.
  - cPCI-6920D is a commercial product that has been known as of the best performance of Blade PC for comactPCI currently.

< cPCI-6920D >

- 2x Quad-Core Intel Xeon LV Processors
- Four SO-RDIMMs for up to 8GB REG/ECC memory
- Four PCI-Express Gigabit Ethernet ports
- 64bit/66MHz PMC/PCI-Express x8 XMC
- Onboard SATA HDD, CompactFlash and USB NAND flash storage
- Dimension : 233.35mm x 160mm x 40mm

- Structure of Implemented System

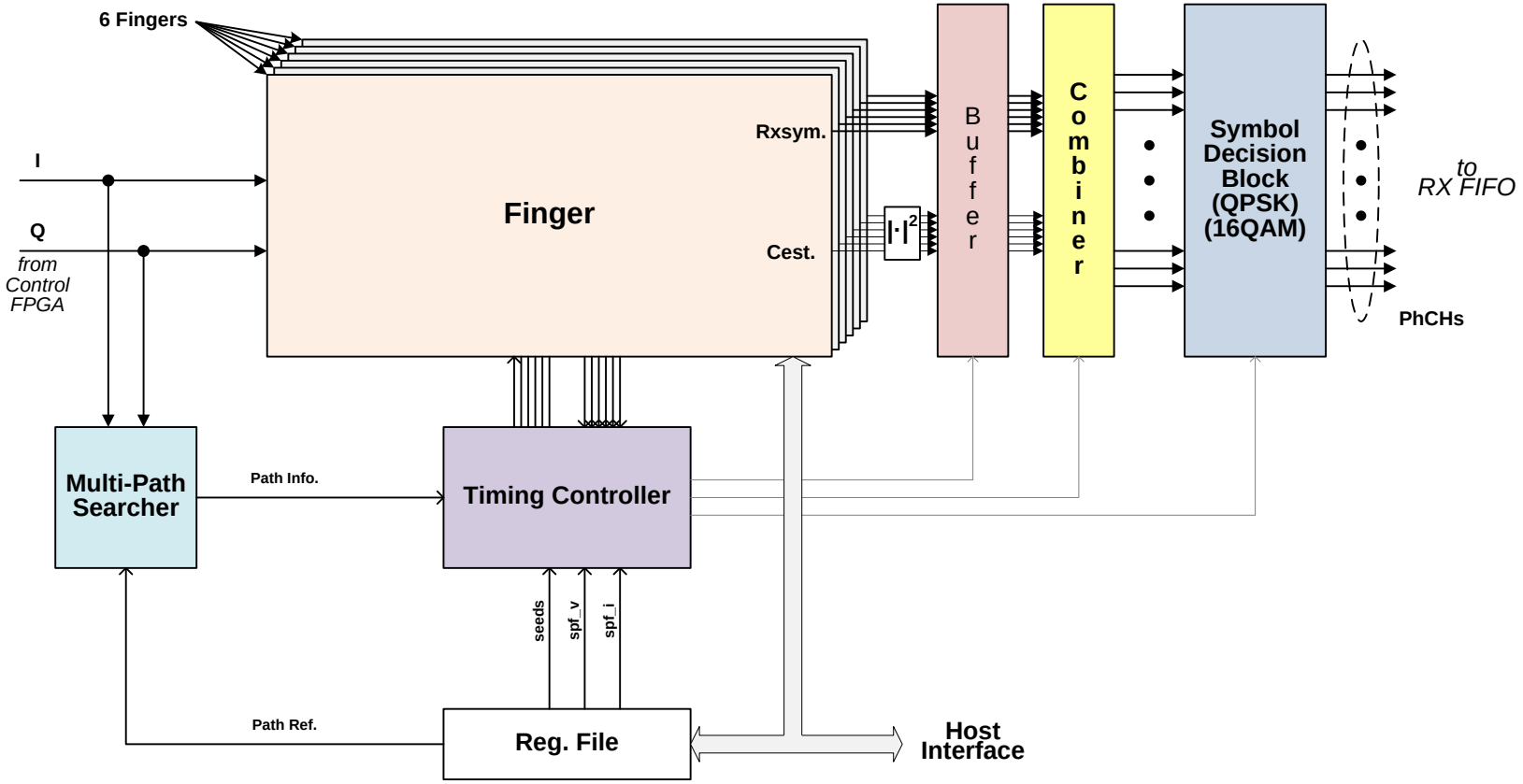
- Implemented Air Protocol Analyzer system and Process Unit



- Algorithm of Physical Layer

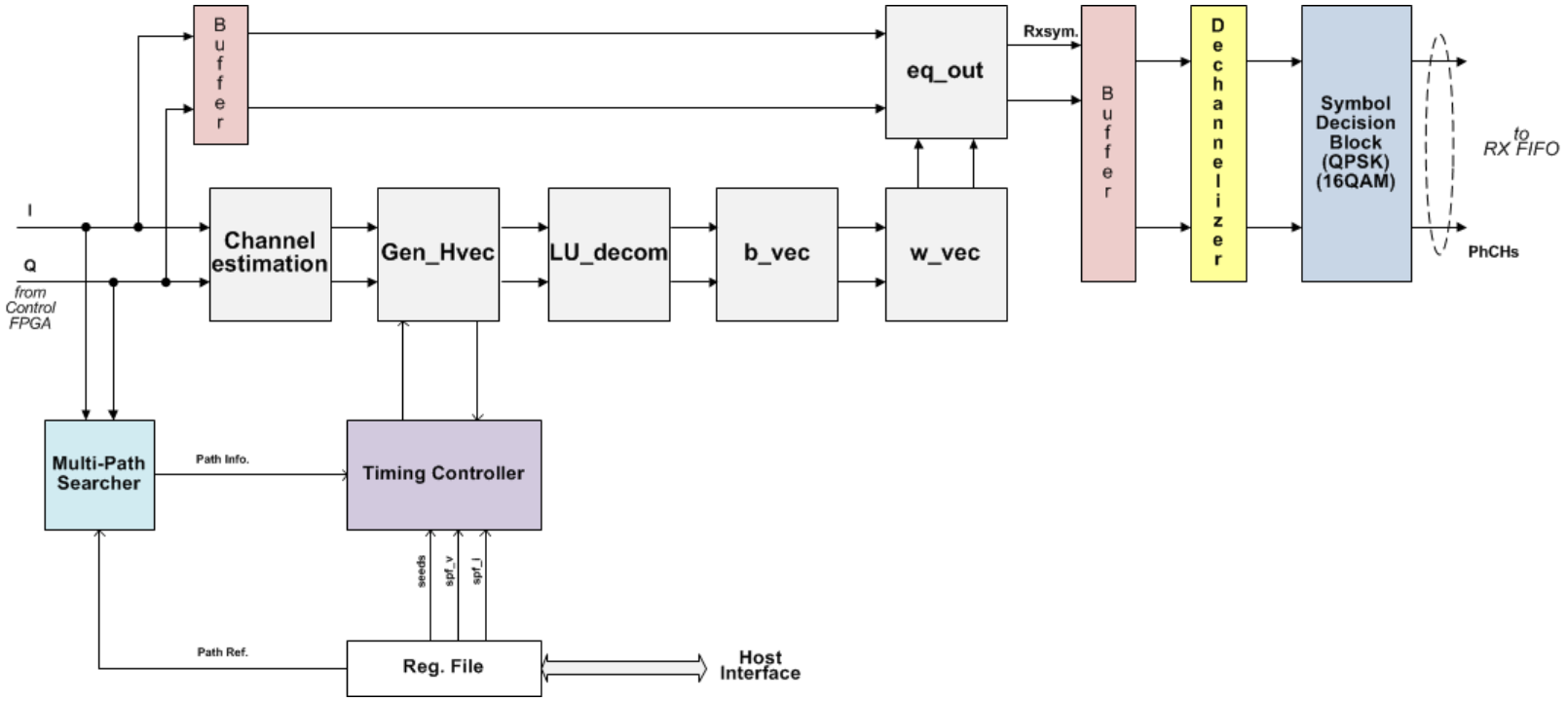
- We consider two receiving algorithms for physical layer data processing, i.e., rake and equalizer.

- Rake receiver



- Algorithm of Physical Layer

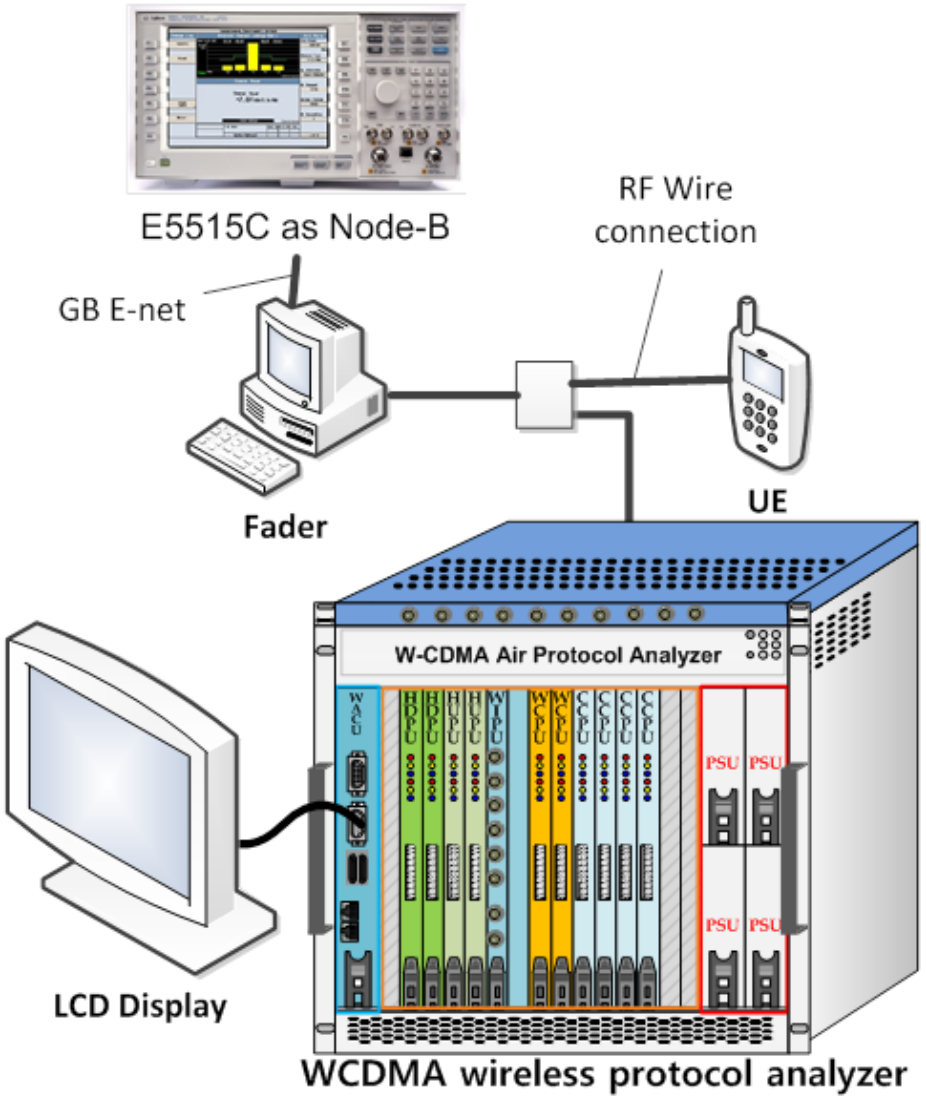
- Equalizer



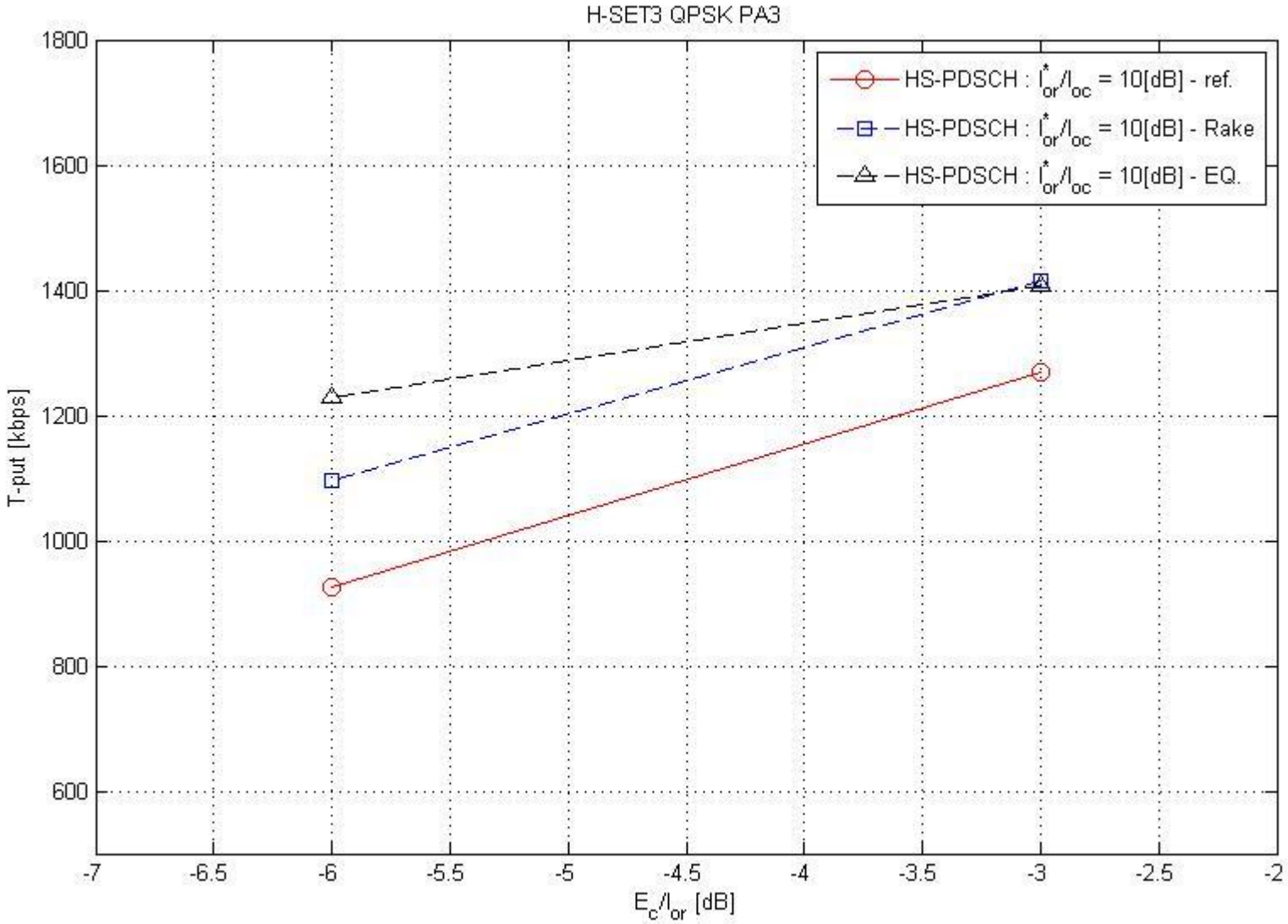
- we have chosen Linear Minimum Mean Square Error (LMMSE) equalizer that uses the inverse of channel matrix.

- Performance Analysis

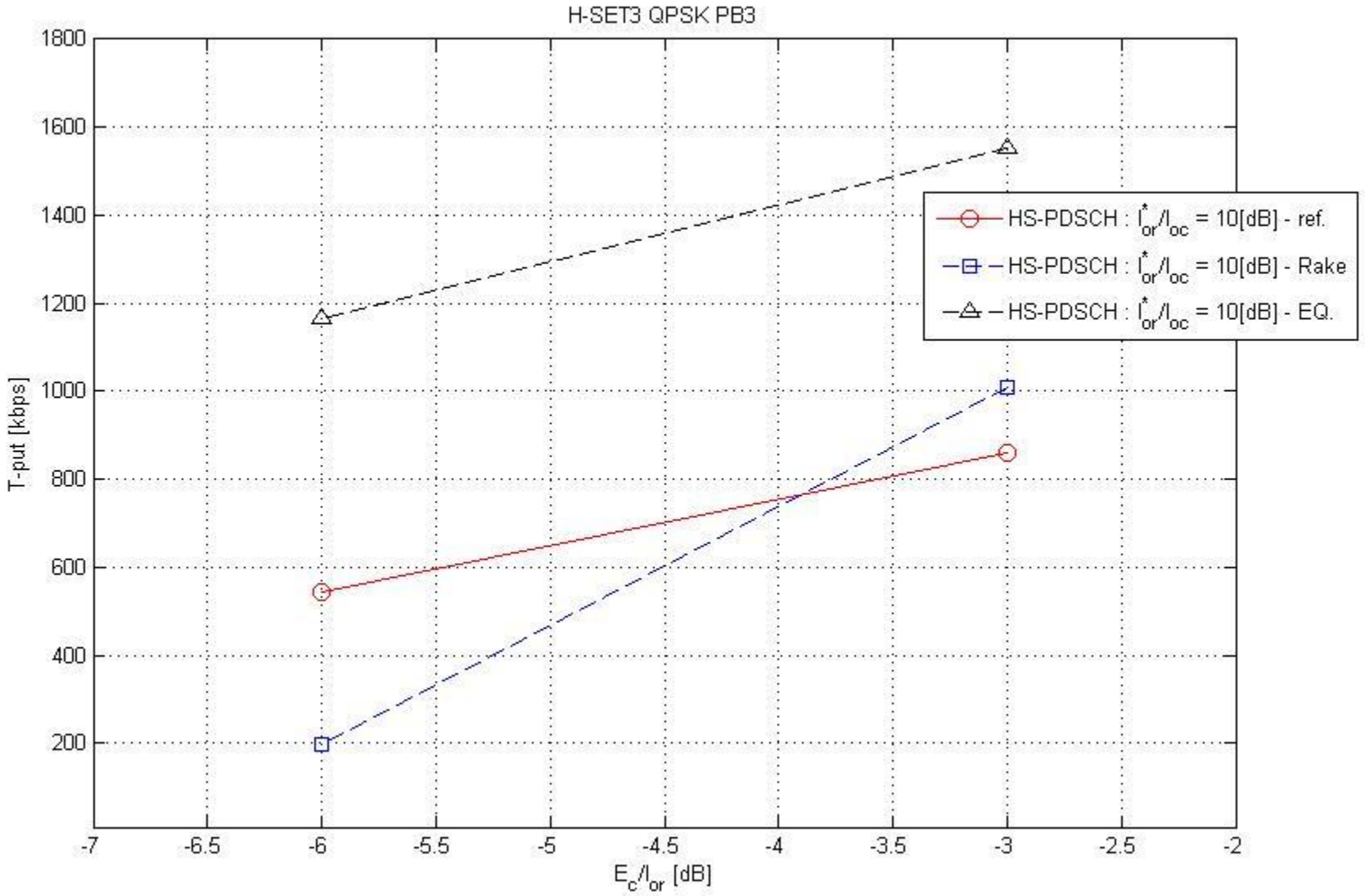
- Experimental Environment
  - Using Agilent E5515C for generating WCDMA/HSDPA/HSUPA signals that are compliant with 3GPP standard.
  - The signal generated from E5515C passes through the fader as shown in figure to be converted into fading signals in accordance with PA3, PB3, VA30, and VA120 that are defined in 3GPP.
- The other parameters
  - - PA3, PB3, VA30, VA120 Multi-path fading Propagation conditions
  - 5 multicodes for QPSK, 4 multicodes for 16QAM
  - Pilot symbol SF = 256
  - Data symbol SF = 16
  - TMS6415 Turbo decoder



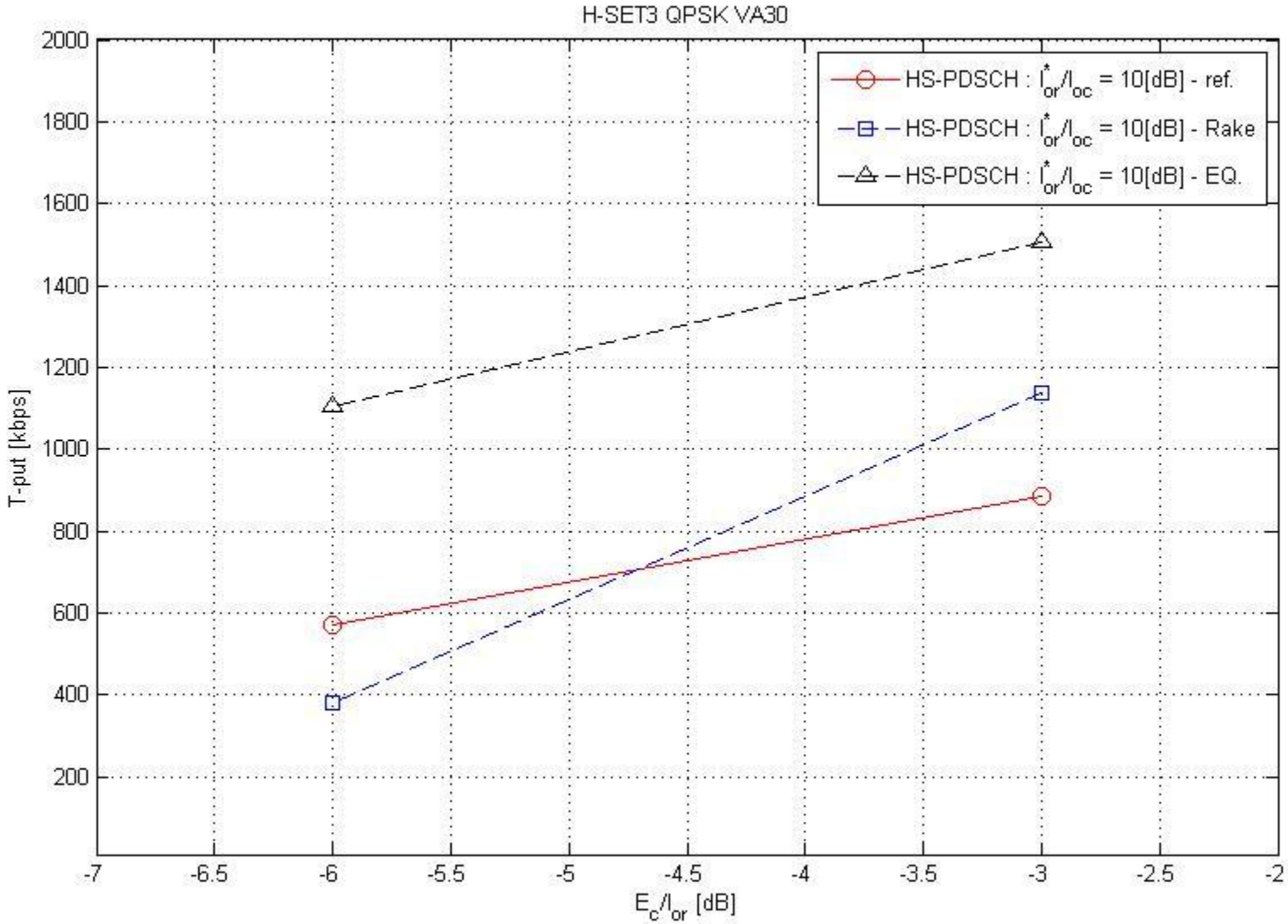
- Performance Analysis(QPSK PA3)



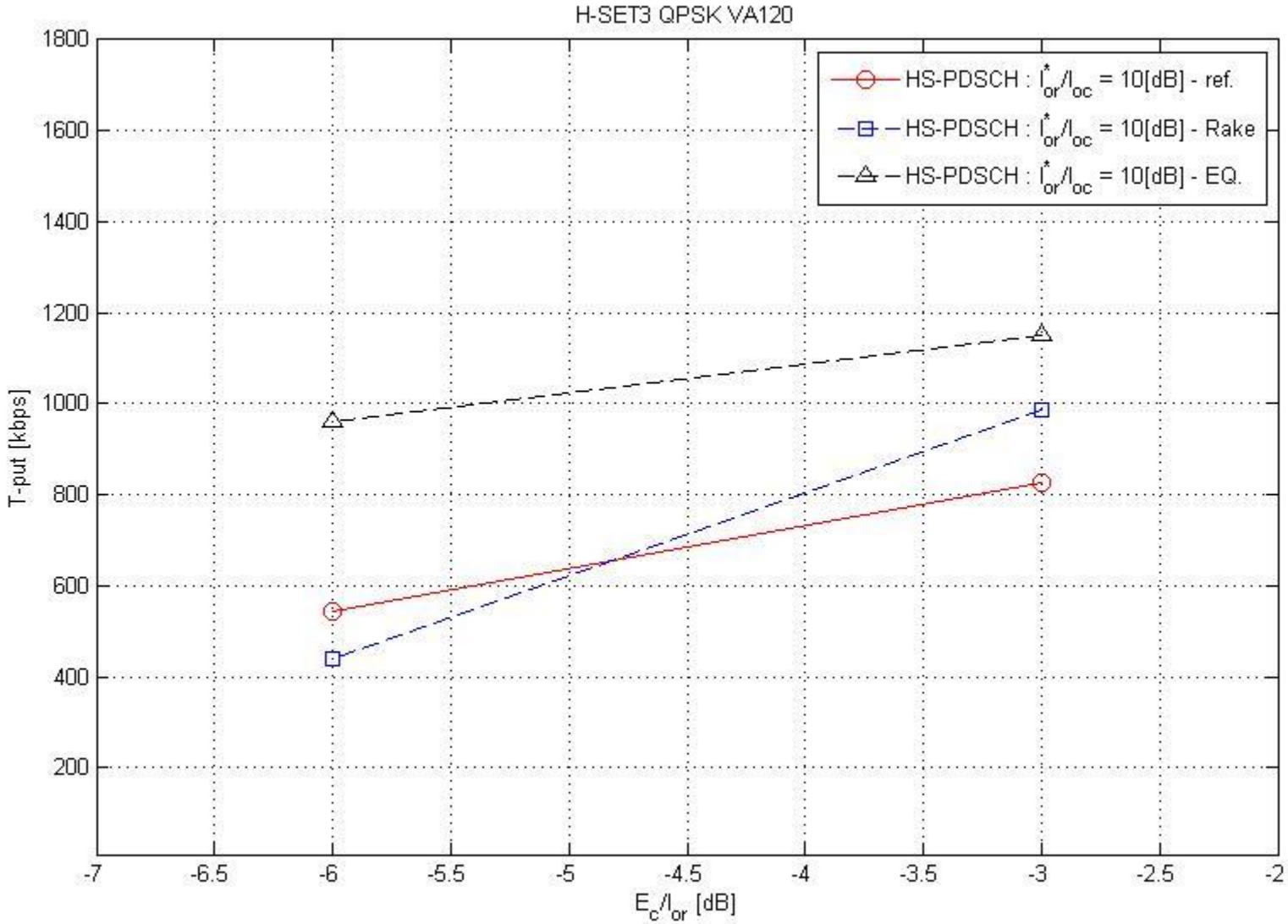
- Performance Analysis(QPSK PB3)



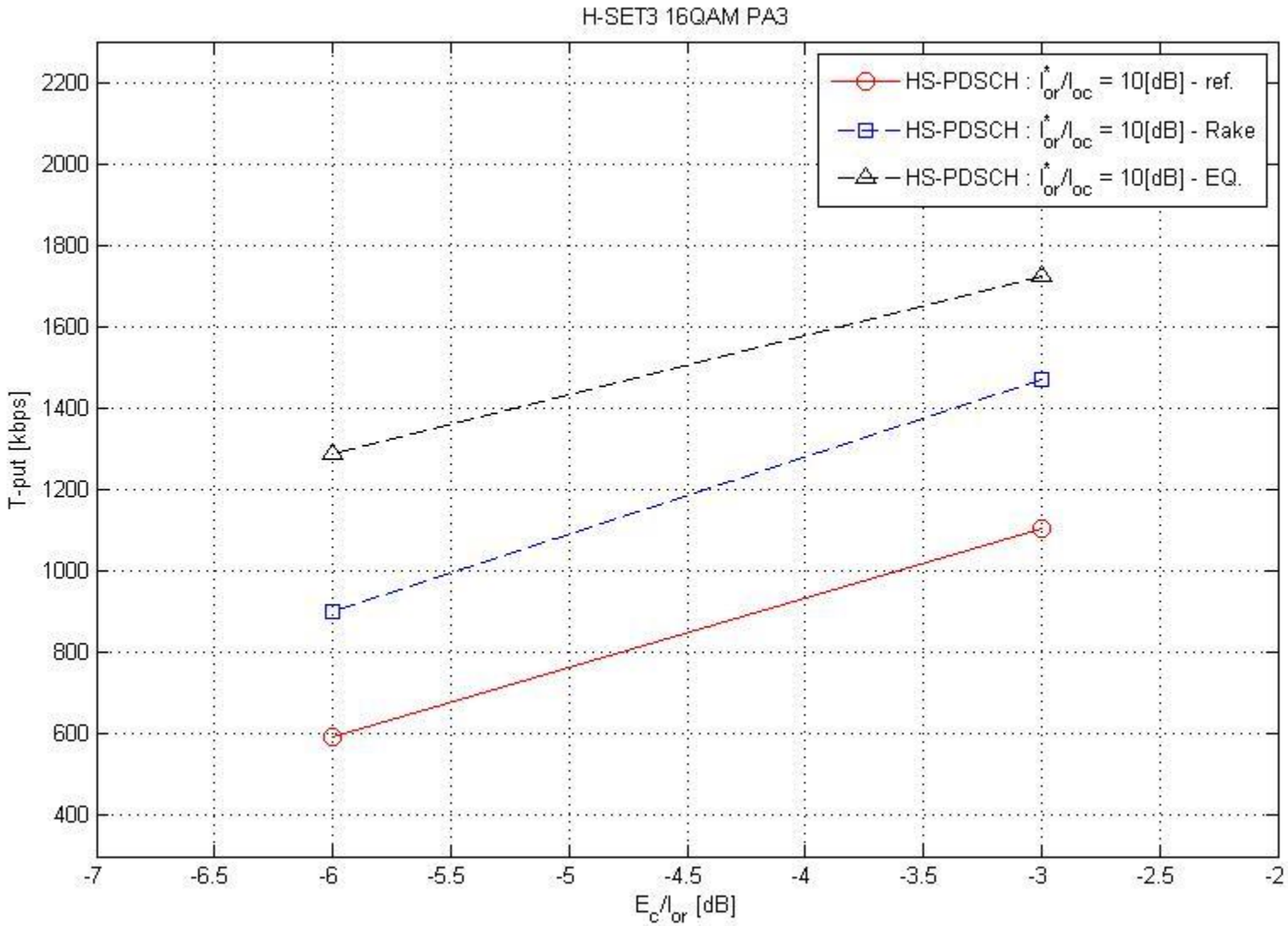
- Performance Analysis(QPSK VA30)



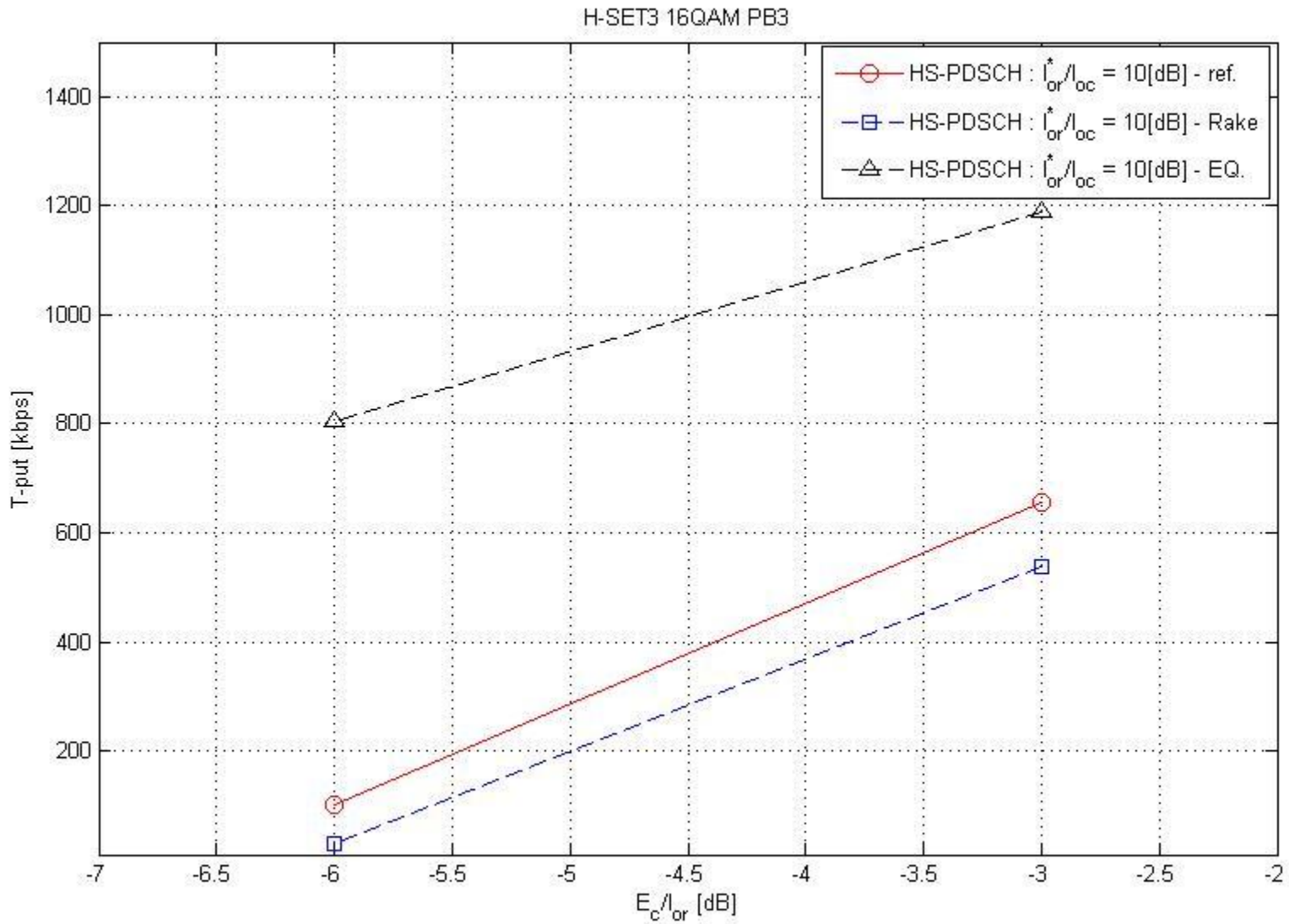
- Performance Analysis(QPSK VA120)



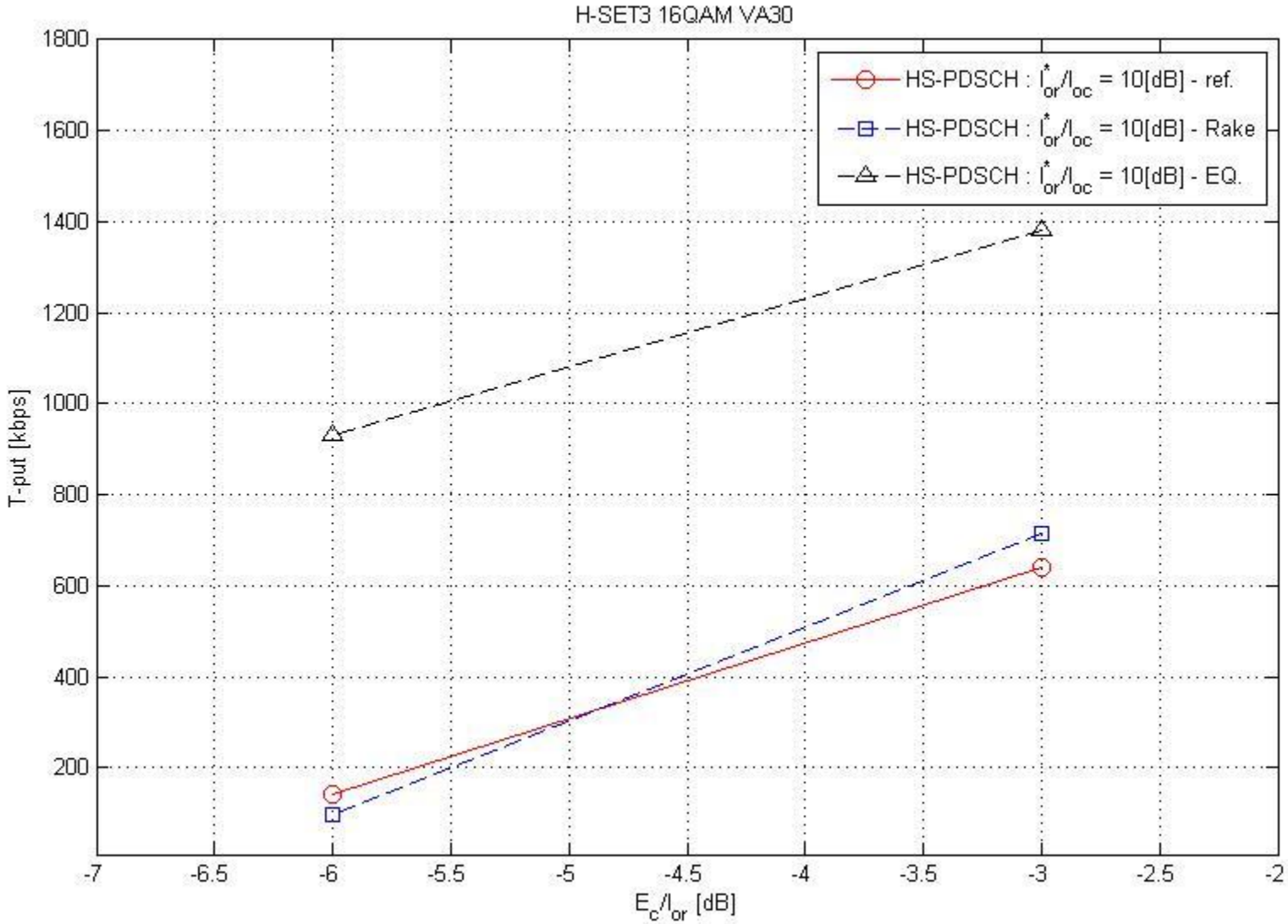
- Performance Analysis(16QAM PA3)



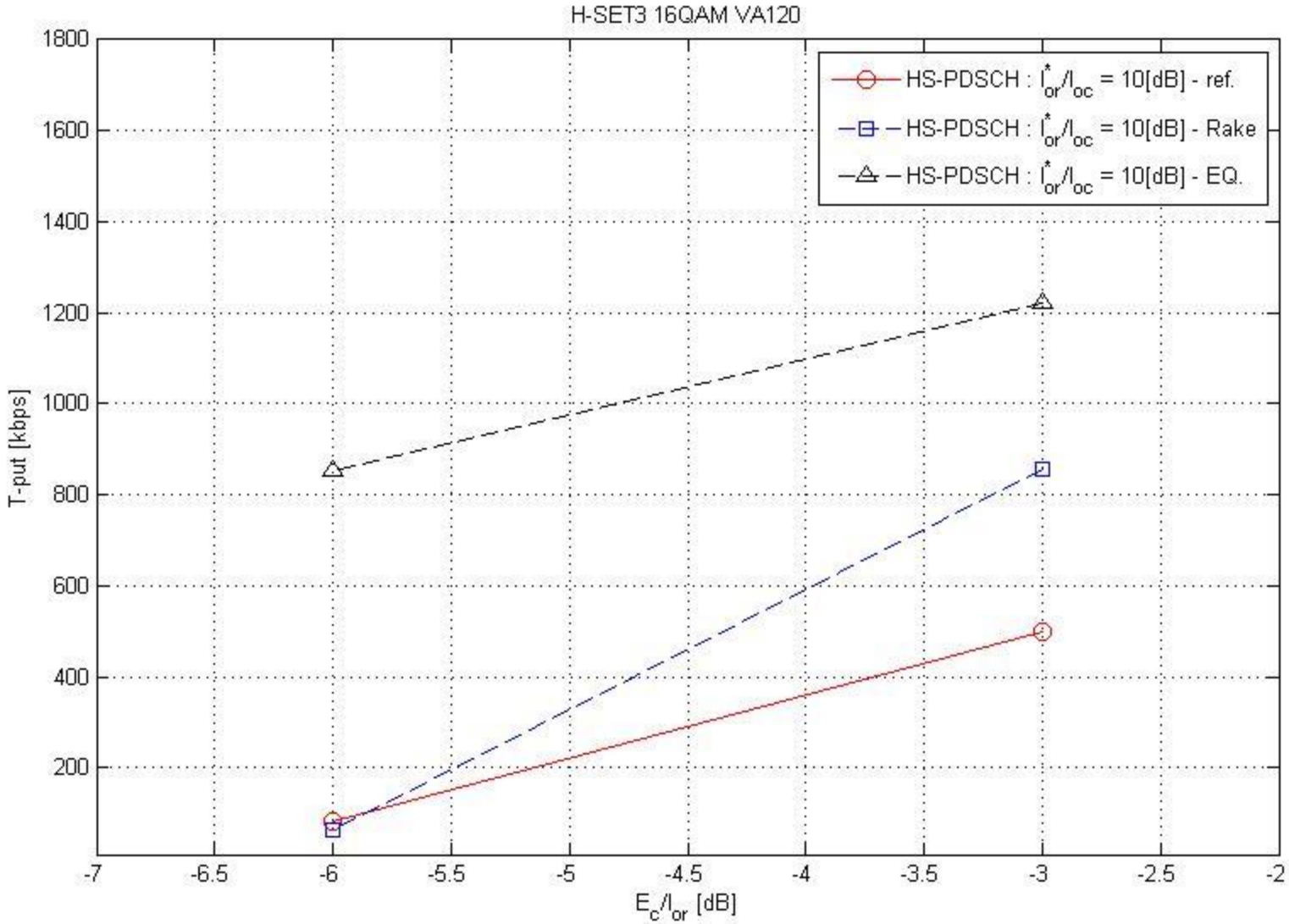
- Performance Analysis(16QAM PB3)



- Performance Analysis(16QAM VA30)



- Performance Analysis(16QAM VA120)



- Conclusion

- we showed an implementation of wireless protocol analyzer designed in SDR-architecture consisting of standard DSPs and FPGAs.

- our system includes L1/L2/L3 decoder, it can capture voice and/or video data of the target UEs..

- We will further extend our system such that it can be reconfigured with LTE and/or Mobile WiMAX by exchanging the S/W of Processing Units.