IMPLEMENTATION OF SDR-BASED WCDMA AIR PROTOCOL ANALYZER WITH AN EQUALIZER FOR SOFTWARE MODEM

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ABSTRACT

This paper presents an implementation of SDR-based Air Protocol Analyzer(APA). APA is a measurement system providing a real-time analysis of wireless signals between User Equipment (UE) and Node-B. It particularly means that the proposed system can capture the wireless signals between UE and node-B from a remote site. Since the implemented system proposed in this paper consists of Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs), it can be reconfigured through a software exchange for supporting various communication standards. The waveform of Wideband Code Division Multiple Access (WCDMA) has been selected for verification of the proposed system, which simultaneously supports up to 48 users in the frequency band of 3 Frequency Allocations (FA) in real-time. In WCDMA system, receiving procedures except some of the Physical (PHY) layer parts, i.e., transport layer part, Layer(L) 2, and L3 parts, are simply reverse of the transmitting procedures like in most other systems as well. So, it could be said in some sense that the entire performance is largely dependent upon PHY layer algorithms. Based on that principle, we designed the software modem using 2 different ways, one with rake method and the other equalization method, to compare the performance to each other. Our experimental tests have shown that throughput provided by equalizer-based modem is nearly 2-10 times higher than that provided by rake-based modem.

1. INTRODUCTION

This paper introduces an implementation of SDR-based wireless protocol analyzer designed by our laboratory. The proposed system adopts standard DSPs and FPGAs for composing its processing units. WCDMA Release 7 has been selected as the target waveform of our SDR-based wireless protocol analyzer. In order for the analyzer to be able to decode the transmit signals and retrieve the original messages in real-time, all the physical, transport, and logical channels defined in 3GPP[1-6] including control and data channels should be decoded exhaustively. It also means that the received signals should be decoded in every layer including Layer(L)1[1-3], L2[4], and L3[5-6] as well. Especially, for the physical layer, we considered the method of rake reception and equalization to compare the performance of each method to each other. In general, equalizer has been known to exhibit a better receiving performance compared to the rake. However, the equalizer-based receiver suffers from a heavier computational burden compared to the rake receiver. In order to resolve the problem of excessive computational load in the equalizer-based receiver, we have adopted a novel procedure of reducing the complexity and computational load[7].

This paper consists of the following sections. Section2 introduces the implemented system of wireless protocol analyzer. Section 3 introduces a novel procedure of reducing the operational complexity associated with the equalizer-based receiver. In Section 4, overall system performance is shown, while Section 5 concludes this paper.

2. STRUCTURE OF IMPLEMENTED SYSTEM

Figure 1 illustrates a block diagram of hardware structure of the implemented WCDMA wireless protocol analyzer. As shown in the figure, the hardware platform of our implemented system consists of Digital Signal Process Units(PUs), Intermediate Frequency(IF) Process Unit(IPU), and Control Unit(CU), which are all composed of plural DSPs and FPGAs. Function of PU includes phase and code synchronization of digital data received from IPU, demodulation of physical channels, demultiplexing for transport channels, and channel coding and error correction. CU performs the following functions: control the status of PU and transfer the transport data demodulated in PU into L2/L3. In addition, CU also

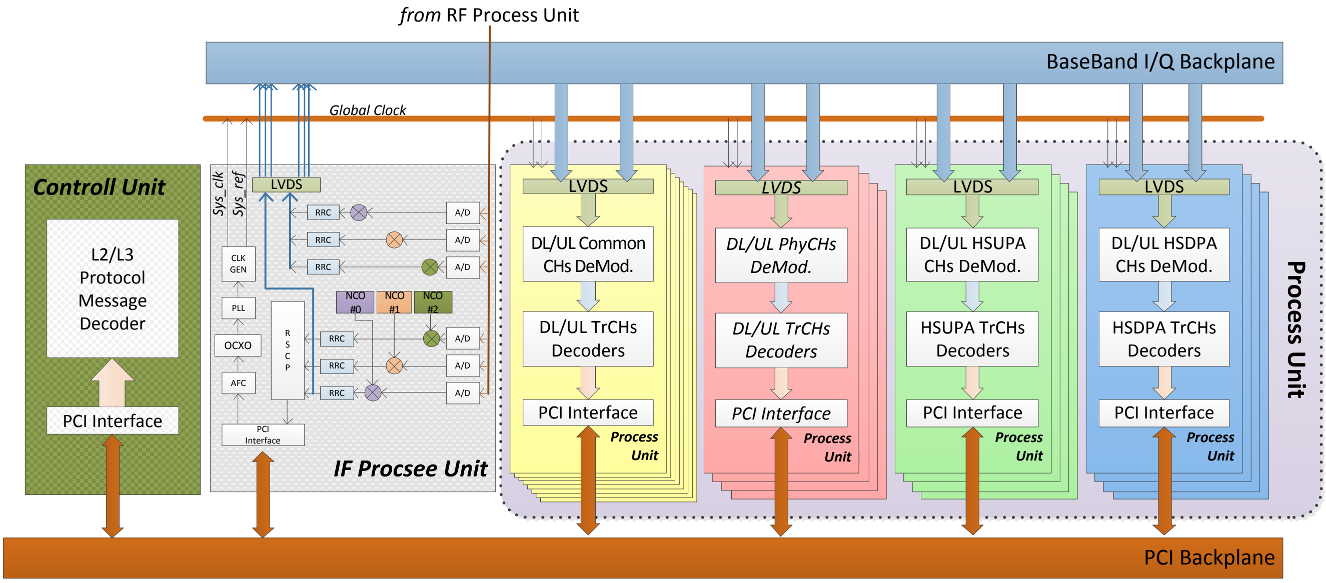

Figure 1. Hardware architecture of implemented WCDMA wireless protocol analyzer

outputs the final decoded data of voice and video signals to the speaker and monitor, respectively. IPU converts the analog IF signals received from Radio Frequency(RF) Process Unit (RPU) into IF digital signals in order to transfer it into each corresponding PU. Furthermore, IPU also stores the IF digital signals in an internal memory for the stored data to be decoded later in off-line processing. Our system can store the IF signal up to 9 hours for the off-line processing. As shown in the upper part of Figure 1, PUs and CUs are sharing the interface of Peripheral Component Interconnect(PCI) in the back plane. Through that interface, up- and down-link signals, decoded transport channel data, and other control signals can be transferred properly. Figure 2 illustrates the hardware structure of PU which consists of 3 FPGAs and 3 DSPs. Table 1 shows how each of conventional interfaces is associated with each of devices in our implemented system. As shown in Table 1, each device is interconnected with each other through a proper conventional interface such that various kinds of signal flows can be supported for various kinds of other waveforms as well as WCDMA which is supported by our implemented system. Devices used in the PU and corresponding interface are summarized in Table 1.

Inscription	Device	Interface
Control FPGA	Cyclone III	LVDS,PCI
FPGA	Stratix IV	LVDS, EMIF
Control DSP	TMS320C6416	EMIF,HPI
DSP	TMS320C6455	EMIF,HPI,PCI

Table 1. PU devices and associated interfaces

It is noteworthy that the implemented system can be reconfigured with any of various kinds of waveforms by downloading the corresponding software modem codes

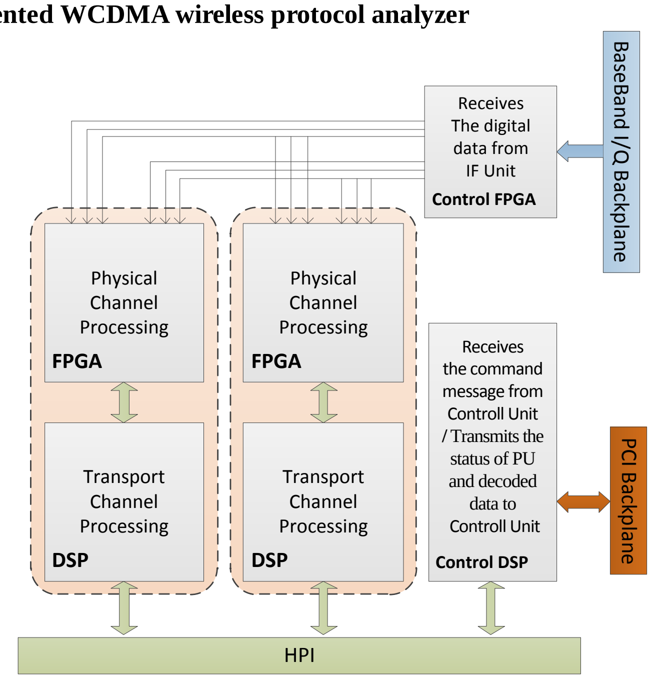

Figure 2. Hardware architecture of PU

into the DSPs and FPGAs in PU, IPU, and/or CU of our system assuming that RPU can handle the frequency band of desired waveforms. Although we considered WCDMA only in this work, we will further extend our system to Long term Evolution(LTE), Mobile-Worldwide Interoperability for Microwave Access (WiMAX), etc. in a near future[8]. Figure 3 is the photograph of implemented system with each unit specified separately.

3. ALGORITHM OF PHYSICAL LAYER

As mentioned earlier, we consider two receiving algorithms for physical layer data processing, i.e., rake and equalizer. Rake-based receiver computes the received signal energy at each of multi-paths in order to separate

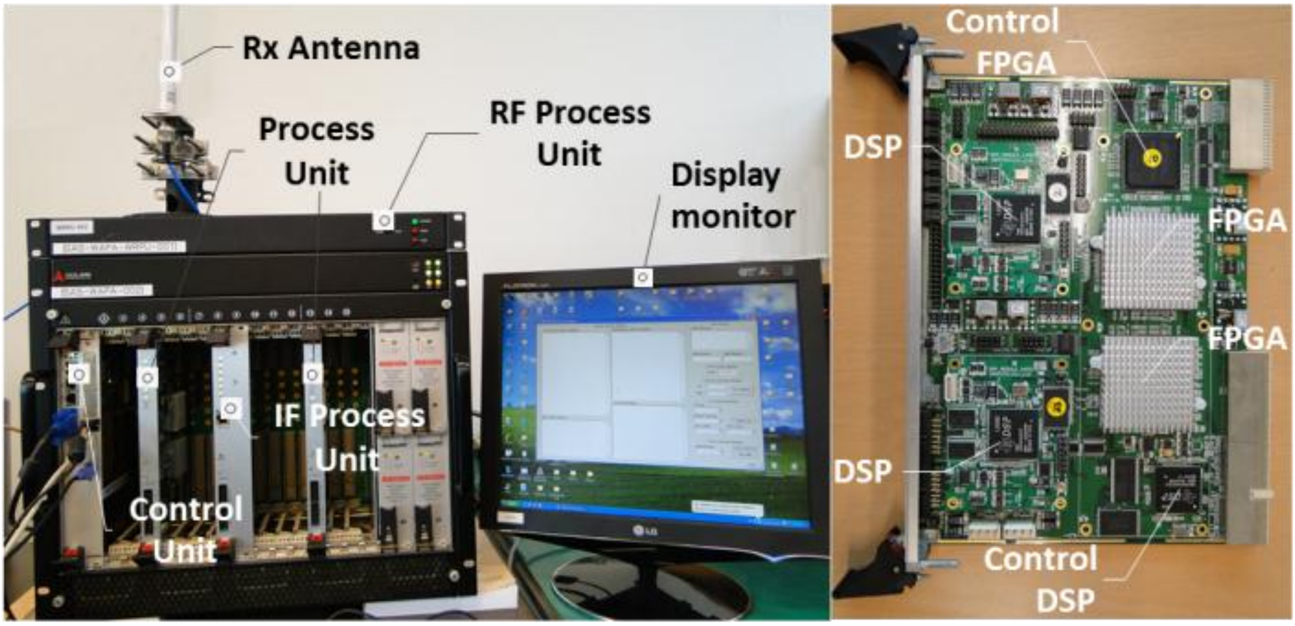

Figure 3. Implemented Air Protocol Analyzer system and Process Unit

each path. Then, decoded symbol is obtained for each of the multi-paths which are often referred to fingers. The symbols are combined using the principle of Maximum Ratio Combining(MRC) [9-10]. When symbol energy is large enough due to a large enough Spreading Factor(SF), rake receiver provides a good performance. When SF is not large enough as in the cases of High Speed Downlink Packet Access(HSDPA) or High Speed Uplink Packet Access(HSUPA), however, rake cannot help suffering a poor performance. Especially, for 16QAM which is very sensitive with environmental adverseness, rake is often found to be unacceptable. On the other hand, since the basic principle of the equalizer-based receiver is to reverse the communication channel, meaning that the interferences due to the low SF is mitigated by the equalizer coefficients that reverse the channel characteristics. Indeed, the equalizer parameters are the reciprocal of channel matrix. Among various algorithms of designing the equalizer, we have chosen Linear Minimum Mean Square Error (LMMSE) equalizer that uses the inverse of channel matrix. Since the LMMSE equalizer uses the inverse channel matrix, it suffers from a large amount of computational load, while it outperforms most conventional equalizers. In this paper, we introduce an efficient procedure of reducing the computational load required by LMMSE equalizer-based receiver[8]. As shown in [8], estimated channel should be input to the equalizer, which means channel parameters should be estimated first in order to adopt equalizer in a given receiver. In our system, we inserted channel estimation values in a preset period of time at every half-chip sampling interval. It particularly means that we need to estimate the channel at a lot more number of sampling time in addition to the ones provided by the searcher and tracker in a rake receiver. Then, we adopted a novel finger-managing algorithm in order to prevent a merge of adjacent fingers. As a merge protection, we deleted overlapped channel parameter if two parameters are located by less than a single chip duration. As for the procedure of computing the inverse of channelmatrix, we have adopted cholesky-factorization, noting that the

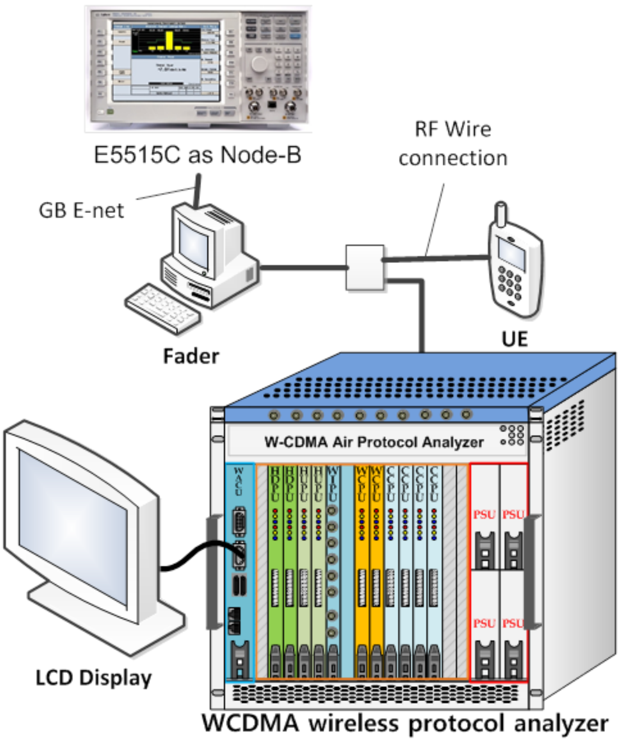

Figure 4. Experimental Environment

Modulation	Channel condition	Hs_PDSCH_Ec (dB)	I^or/Ioc (dB)	3GPP Ref. 25.101 (kbps)	Rake_T-put (kbps)	LMMSE_EQ T-put(kbps)
QPSK	PA3	-6	10	927	1096.7	1229.6
	PA3	-3	10	1269	1415.3	1407.3
	PB3	-6	10	543	197.7	1167.1
	PB3	-3	10	861	1008.0	1551.4
	VA30	-6	10	570	380.1	1027.8
	VA30	-3	10	885	1136.8	1445.7
	VA120	-6	10	543	438.0	869.3
	VA120	-3	10	825	987.3.	1397.7
16QAM	PA3	-6	10	594	899.9	1287.3
	PA3	-3	10	1104	1470.6	1723.3
	PB3	-6	10	102	29.8	1056.4
	PB3	-3	10	657	538.5	1490.1
	VA30	-6	10	141	97.5	1005.1
	VA30	-3	10	642	715.0	1380.5
	VA120	-6	10	84	64.8	874.5
	VA120	-3	10	501	856.5	1187.0

Table 2. Test results of performance analysis using E5515C as node-B

channel matrix is quasi-toeplitz matrix. Since the channel matrix is sparse matrix, cholesky-factorization brings a lot of computational saves. More specifically, when processing cholesky-factorization, we caculate the value of the first column only and adopt the same value diagonally, because the channel matrix is sparse. The algorithm is illustrated in Figure 5. Though it causes a miner degradation in performance, it is negligible compared to the gain in computational complexity. Recalling that the computational burden of cholesky-factorization is proportional to the 3rd power of number of equalizer taps, to reduce the number of columns associated with cholesky-factorization tremendously mitigates the computational burden. Exploiting the sparseness and toeplitzness of channel matrix, we have reduced the computational burden of cholesky-factorization effectively by a factor of 2nd power of equalizer taps because we adopted the same value obtained from the first column to all the other values for the other columns. The equalizer adopts max 12 bit and truncate the sub 10 bit.

4. Performance Analysis

This section compares the performance of rake-based receiver to the equalizer-based receiver in WCDMA various signal environments. Figure 4 illustrates our experimental environment which consists of AgilentE5515C, fading emulator, test UE, power divider, and our wireless protocol analyzer together with a

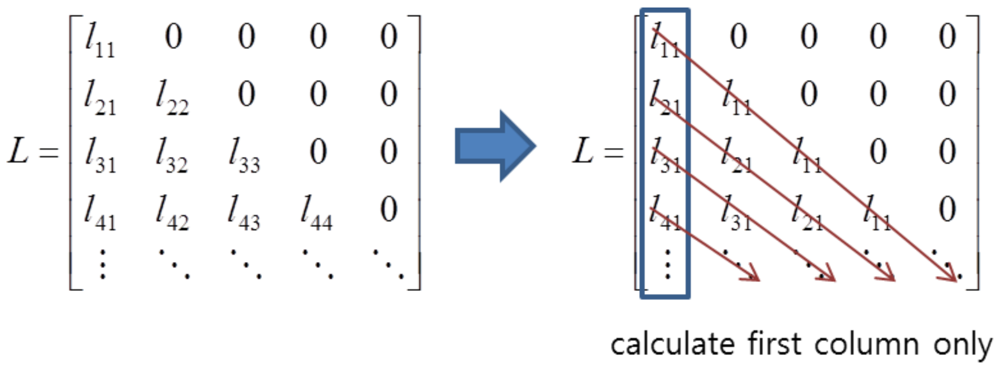

Figure 5. Explanation of proposed Cholesky-factorization

monitor. We have also performed performance analysis in real environments where the target UE is communicating with its node-B while our wireless protocol analyzer captures the wireless signal from remote site. In this work, we present the results of Agilent E5515C-based laboratory tests only. Agilent E5515C generates WCDMA/HSDPA/HSUPA signals that are compliant with 3GPP standard. In other words, E5515C is a base station emulator. The signal generated from E5515C passes through the fader as shown in Figure 4 to be converted into fading signals in accordance with PA3, PB3, VA30, and VA120 that are defined in 3GPP[11]. The fading signals generated with E5515C and fader are applied to both test UE and our wireless protocol analyzer. Throughput obtained by the rake-based and equalizer-based receiver are compared to each other. The other parameters in the experimental tests are as follows:

- PA3, PB3, VA30, VA120 Multi-path fading Propagation conditions
- 5 multicodes for QPSK, 4 multicodes for 16QAM
- Pilot symbol SF = 256
- Data symbol SF = 16
- TMS6415 Turbo decoder
- LMMSE equalizer with 60 tap(4 oversample),
- Rake receiver with 6 fingers

Test results obtained from the implemented system are shown in Table 2.

As shown in the table, since PA3 environments is associated with the shortest channel dispersion, merits of equalizer are not seen conspicuously. However, for the other signal environments especially for PB3, equalizer outperforms the rake receiver which is even under the requirements of 3GPP regulation specified in 3GPP TS.

5. Conclusions

In this paper, we showed an implementation of wireless protocol analyzer designed in SDR-architecture consisting of standard DSPs and FPGAs. WCDMA Release 7 has been chosen for a target waveform of the implemented system while the target waveform could be determined arbitrarily using the same hardware baseband signal processing platform. The implemented system retrieves the transmitted information in either real-time or off-line processing of storage data. The wireless protocol analyzer can capture the wireless signal from remote site for up to 16 target UEs while each UE can communicate with one of 8 node-Bs. Since our system includes L1/L2/L3 decoder, it can capture voice and/or video data of the target UEs. Amongst many signal processing algorithms, we considered 2 typical baseband signal processing algorithms, rake and equalizer. As equalizer far outperforms the rake, we have developed a novel method of reducing the computational load for designing the equalizer based on LMMSE. According to our equalizer, which is 4 times oversampled with 60 taps, our wireless protocol analyzer satisfies all the requirements specified in 3GPP TS 25.101 for various signal environments such as PA3, PB3, VA30, and VA120. It is noteworthy that the required computational load has been reduced from 3rd order to 2nd order of tap number by exploiting the sparseness and toeplitzness of the channel matrix. Although we have presented the results of laboratory tests only, we conclude that our SDR-based wireless protocol analyzer is fully compliant with the requirements of target waveform which is WCDMA in this work. We will further extend our system such that it can be reconfigured with LTE and/or Mobile WiMAX.

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