Low-Complexity SDR Implementation of IEEE 802.15.4 (ZigBee) Baseband Transceiver on Application Specific Processor

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Outline

- IEEE 802.15.4
- TTA Processor Architecture
- Transmitter and Receiver Design
- Performance Figures
- Conclusion

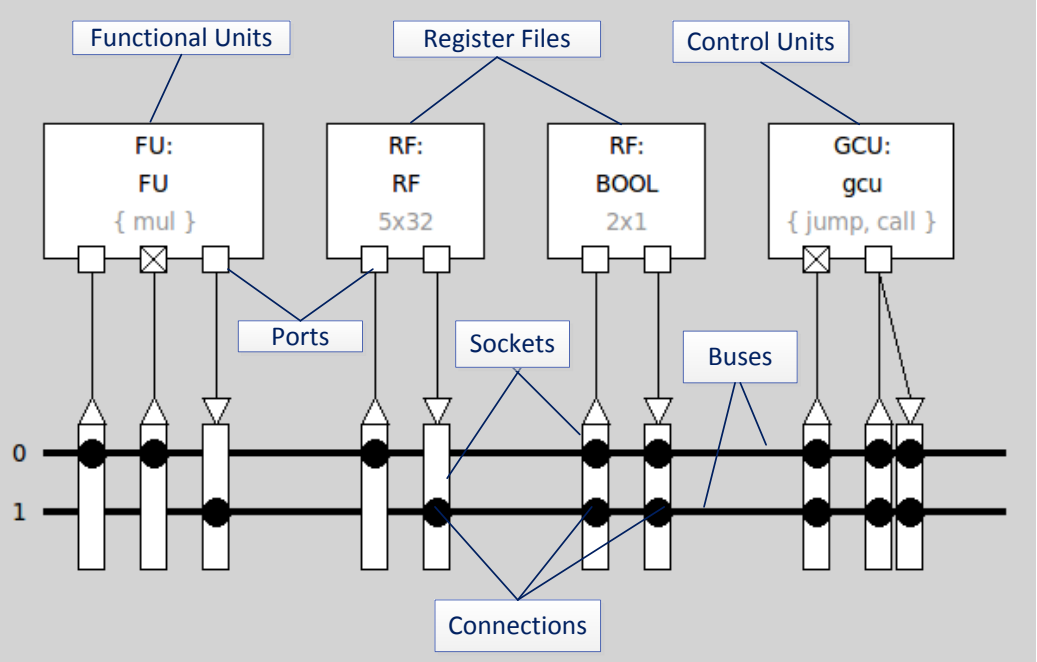
Goals

- Performance analysis of SDR realization on an Application Specific Processor
- Modifying existing reciever algorithms to suit SDR realization
- Designing Application Specific Processor for the implementation of algorithms

IEEE 802.15.4 Standard

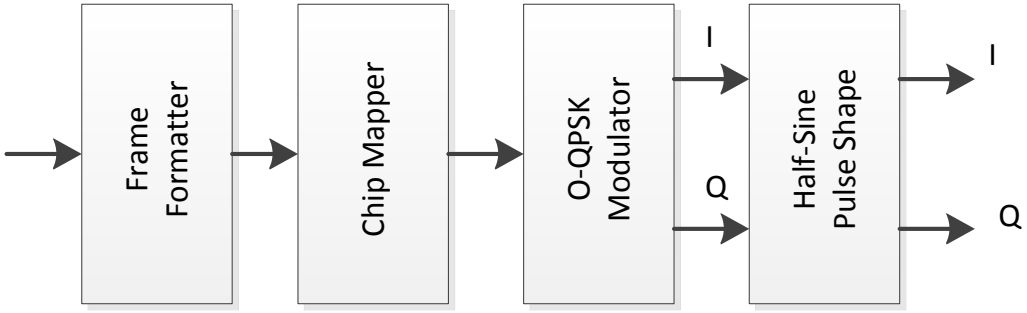
- Low data rate Wireless Personal Area Network (LR-WPAN)
- IEEE provides physical and MAC Layer specifications
- Frequency: 2.4 GHz
- Bit rate: 250 kbps
- Modulation: O-QPSK with Half-sine pulse shape
- Coding: Direct Sequence Spread Spectrum based on 32-bit orthogonal PN sequences

Transport Trigger Architecture (TTA)



- Processor design paradigm where computations happen as side effect of data transport

Transmitter Design

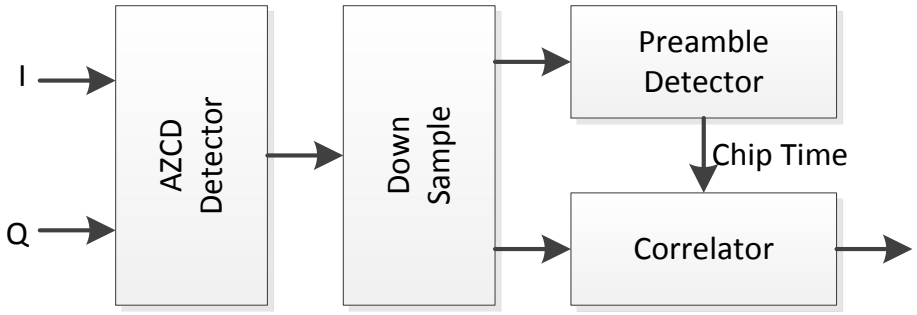


- Frame Formatter: Packet as per the specification
- Chip Mapper: For Direct Sequence Spreading
- O-QPSK Modulator
- Half Sine Pulse Shaper

TTA Processor for Transmitter

- Resources on Processor
  - 2 ALUs
  - 1 LSU
  - 1 GCU
  - 1 FU for Multiplication
  - 4 register files with five 32-bit registers each
  - SFU for serial input and output of data
  - 6 data Buses
- Gate Count Estimate: 16k

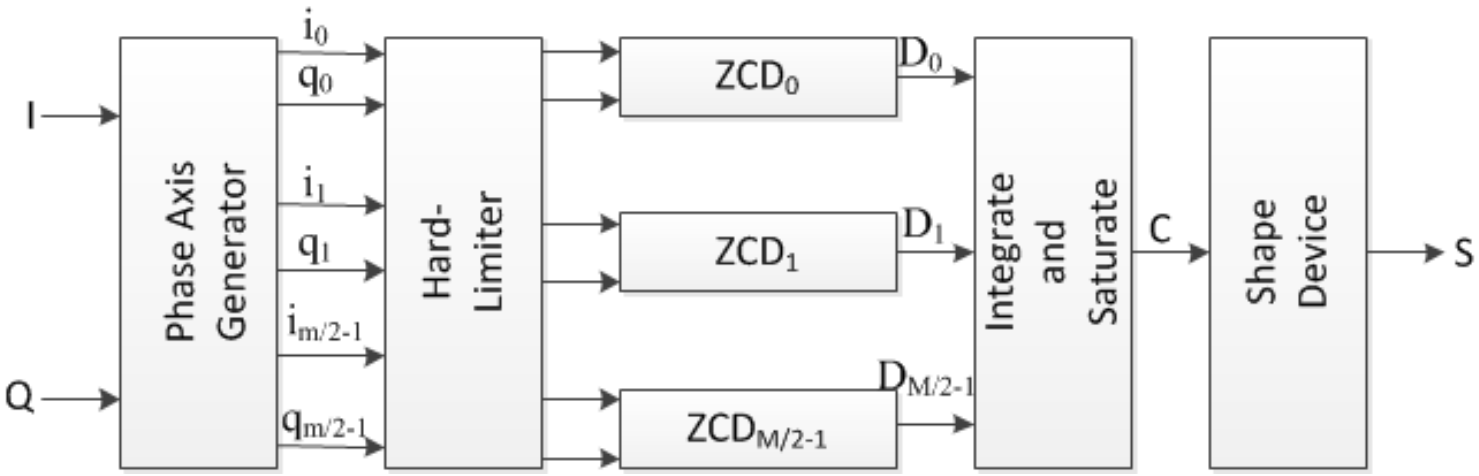
Receiver Design



- Non-coherent Detection
  - Based on Asynchronous Zero Crossing Detector (AZCD)
  - MSK interpretation of O-QPSK with Half sine Pulse Shape
  - Phase and timing synchronization not needed
  - Easy to implement on low power and low cost devices

Rx Design...

- AZCD Detector



  - Number of phase axes: 8

Rx Design…

- ZCD
  - Phase Axis Generation: To work with lower modulation index

$$\begin{cases} i_k = i.\cos\theta_k + q.\sin\theta_k \\ q_k = -i.\sin\theta_k + q.\cos\theta_k \end{cases}$$

  - Zero Crossing Detection: Detects the direction of phase axis crossing for a particular pair of axes

$$D_k = 1/2[i_k.(q_k - q_{k-1}) - q_k.(i_k - i_{k-1})]$$

  - D_k = -1 (clockwise), 1 (Anti-clock), 0 (No crossing)
  - Saturation

$$C_i = \text{sat}(C_{i-1} + D_k)$$

  - Shape Device: $S_i = \begin{cases} S_{i-1} & if\ C_i = 0 \\ C_i & otherwise \end{cases}$

Rx Design..

- Down Sample
  - AZCD algorithm provides shape of the MSK/O-QPSK Coded signal
  - E = Oversampling Factor, M = number of Phase axis
  - Down Sample by E/2 * M/2
- Preamble Detection
  - Correlate incoming signal with preamble chip to detect packet
  - Down sampling done at multiple offset for best preamble correlation (Best chip time)

Rx Design

$$a_k = \mathrm{O} - \mathrm{QPSK}$$
$$d_k = \mathrm{MSK}$$

- Correlator
  - De-spreading of chip sequence
  - Spreading codes encoded with MSK/O-QPSK coding equation

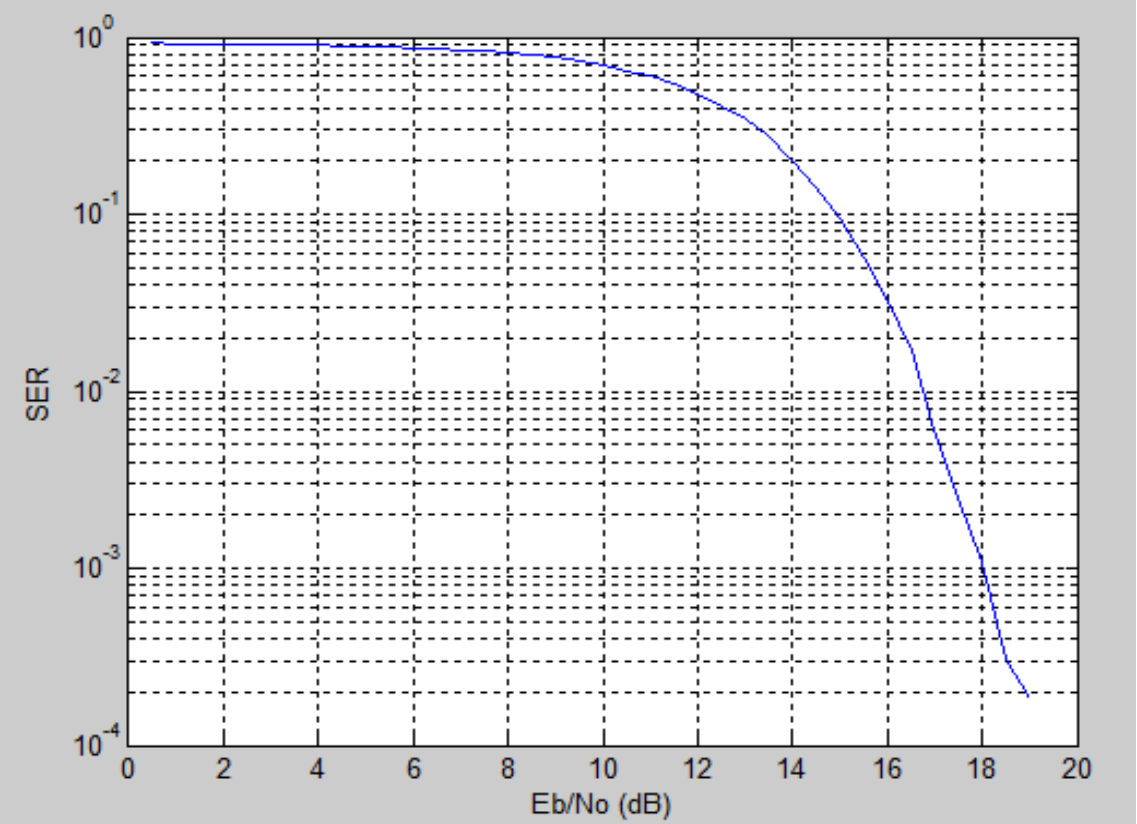
$$\begin{cases} d_{2k} = a_{2k+1} a_{2k} \\ d_{2k+1} = -a_{2k+2} a_{2k+1} \end{cases}$$

  - Detected chips packed in 32-bit memory
  - replace multiply-and-accumulate operation by bitwise XOR and count number of 1s in 32-bit register
  - Least number of 1s => Best correlation

TTA Processor for Receiver

- Resources on Processor
  - 8 ALUs
  - 2 LSU
  - 1 GCU
  - 8 register files with eight 32-bit registers each
  - SFU for serial input and output of data
  - 8 SFU for computing sign of a number
  - 1 SFU for Saturation, 1 SFU for counting 1s
  - 16 data Buses
- Gate Count Estimate: 95k

SER Performance



Required Sensitivity = -85 dBm
Eb/No =19 dB
NF = 7 dB

Performance

- Cycle count for transmitter
  - CPU Cycle = 1088 * PPDU Size (Byte) + 23
  - Clock requirement for 250 kbps = 35 MHz
- Cycle count for receiver
  - 5930 CPU cycles/byte of data
  - Preamble Detection overhead: 32k cycles
  - Clock requirement: 200 MHz

Conclusion

- TTA processors could provide an ideal platform for SDR implementation of low power and low cost wireless standards.
- Data throughput of 250 kbps achieved.

Parameters	System-on-chip	SDR on GPP	SDR on ASP (TTA)
Programmability	No	Yes	Yes
Integration with Sensor Nodes	Yes	No	Yes
Real-time Processing	Yes	No	Yes
Low-Cost	Yes	NA	Yes

- The SER performance of the demodulator is in agreement with IEEE 802.15.4 requirements.
- The processor have low gate count estimates, allowing for a low power and low cost implementation.

Thank You!
Questions?

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